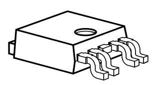
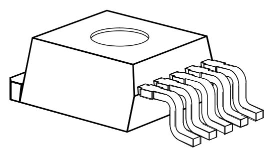
5-V Low-Drop Voltage Regulator — TLE 4275

Features

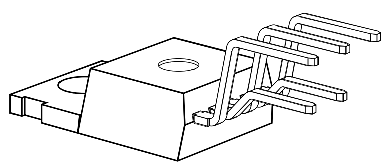
- Output voltage 5 V ± 2%
- Very low current consumption
- Power-on and undervoltage reset
- Reset low down to V_Q = 1 V
- Very low-drop voltage
- Short-circuit-proof
- Reverse polarity proof
- Suitable for use in automotive electronics
- ESD protection > 4 kV



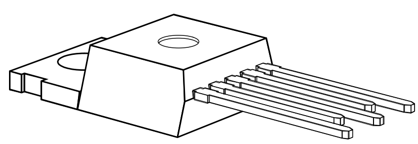
P-TO252-5-1



P-TO263-5-1



P-TO220-5-11



P-TO220-5-12

Type	Ordering Code	Package
• TLE 4275 D	Q67006-A9354	P-TO252-5-1 (SMD)
• TLE 4275 G	Q67006-A9343	P-TO263-5-1 (SMD)
• TLE 4275	Q67000-A9342	P-TO220-5-11
• TLE 4275 S	Q67000-A9442	P-TO220-5-12

• New type

Functional Description

The TLE 4275 is a monolithic integrated low-drop voltage regulator in a 5 pin TO-package. An input voltage up to 45 V is regulated to $V_{Q,nom}$ = 5.0 V. The IC is able to drive loads up to 450 mA and is short-circuit proof. At overtemperature the TLE 4275 is turned off by the incorporated temperature protection. A reset signal is generated for an output voltage $V_{Q,rt}$ of typ. 4.65 V. The delay time can be programmed by the external delay capacitor.

Dimensioning Information on External Components

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating of input inductivity and input capacitance can be damped. The output capacitor C_Q is necessary for the stability of the regulation circuit. Stability is guaranteed at values $C_Q \geq 22\ \mu F$ and an ESR of $\leq 5\ \Omega$ within the operating temperature range.

Circuit Description

The control amplifier compares a reference voltage to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the power element. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Over-temperature
- Reverse polarity

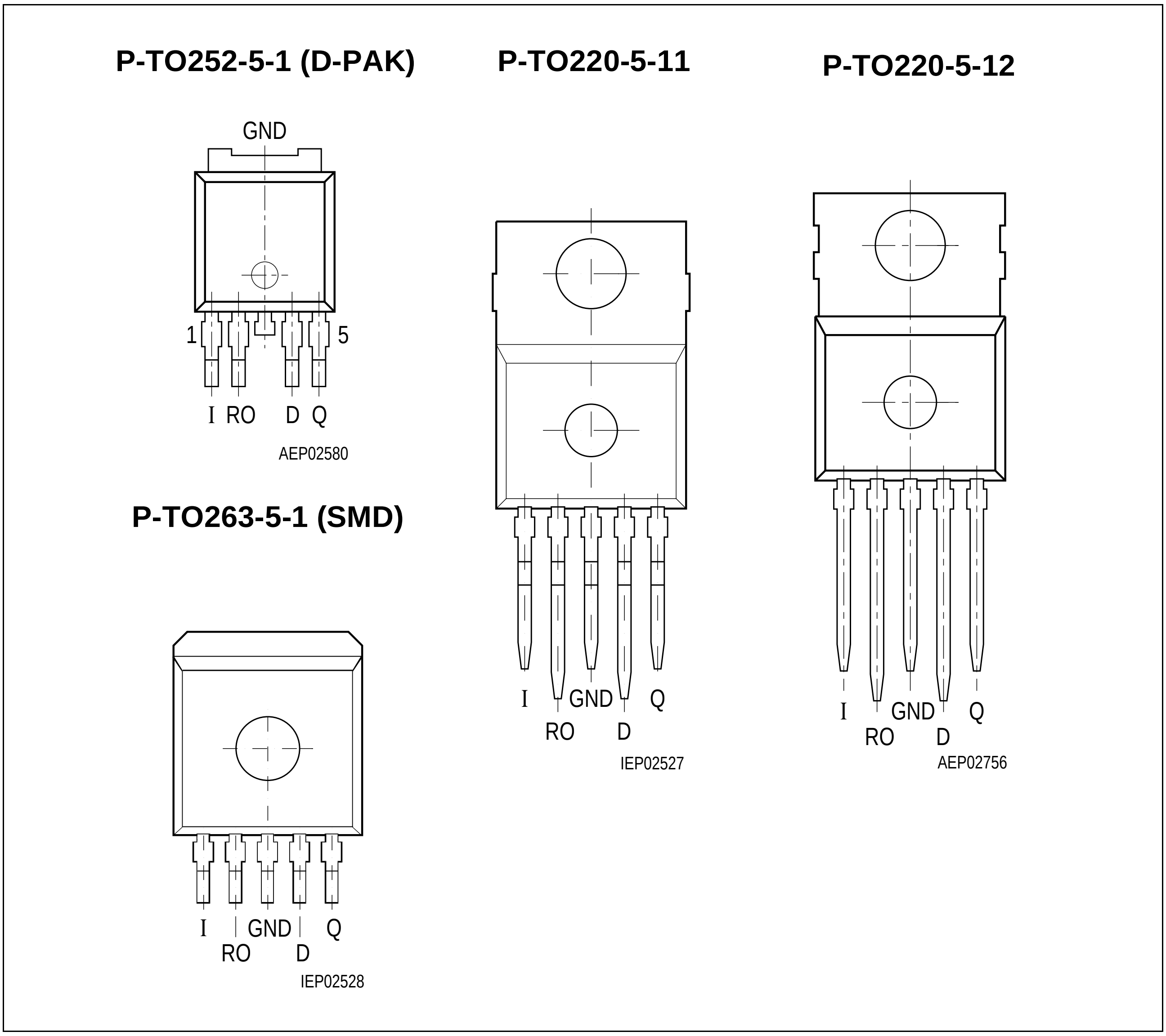


Figure 1 **Pin Configuration** (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	**Input**; block to ground directly at the IC by a ceramic capacitor.
2	RO	**Reset Output**; open collector output
3	GND	**Ground**; Pin 3 internally connected to heatsink
4	D	**Reset Delay**; connect capacitor to GND for setting delay time
5	Q	**Output**; block to ground with a ≥ 22 µF capacitor, ESR < 5 Ω at 10 kHz.

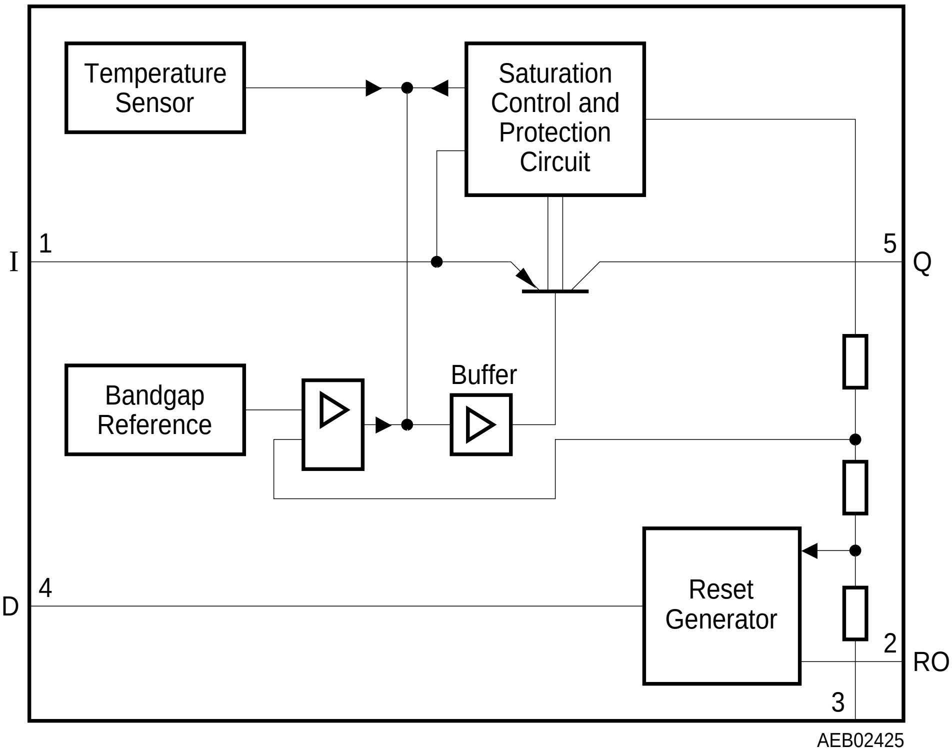


Figure 2 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Voltage Regulator					
Input					
Voltage	V_I	– 42	45	V	–
Current	I_I	–	–	–	Internally limited
Output					
Voltage	V_Q	– 1.0	16	V	–
Current	I_Q	–	–	–	Internally limited
Reset Output					
Voltage	V_{RO}	– 0.3	25	V	–
Current	I_{RO}	– 5	5	mA	–
Reset Delay					
Voltage	V_D	– 0.3	7	V	–
Current	I_D	– 2	2	mA	–
Temperature					
Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input voltage	V_I	5.5	42	V	–
Junction temperature	T_j	– 40	150	°C	–

Thermal Resistance

Junction case	R_{thjc}	–	4	K/W	–
Junction ambient	$R_{thj\text{-}a}$	–	53	K/W	TO263[1)]
Junction ambient	$R_{thj\text{-}a}$	–	78	K/W	TO252[1)]
Junction ambient	$R_{thj\text{-}a}$	–	65	K/W	TO220

1) Worst case, regarding peak temperature; zero airflow; mounted on a PCB FR4, 80 × 80 × 1.5 mm^3, heat sink area 300 mm^2

Characteristics

V_I = 13.5 V; – 40 °C < T_j < 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Output						
Output voltage	V_Q	4.9	5.0	5.1	V	5 mA < I_Q < 400 mA 6 V < V_I < 28 V
Output voltage	V_Q	4.9	5.0	5.1	V	5 mA < I_Q < 200 mA 6 V < V_I < 40 V
Output current limitation[1)]	I_Q	450	700	–	mA	–
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	200	µA	I_Q = 1 mA; T_j = 25 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	150	220	µA	I_Q = 1 mA; $T_j \leq$ 85 °C
Current consumption; $I_q = I_I - I_Q$	I_q	–	5	10	mA	I_Q = 250 mA
Current consumption; $I_q = I_I - I_Q$	I_q	–	12	22	mA	I_Q = 400 mA

Characteristics (cont'd)
V_I = 13.5 V; – 40 °C < T_j < 150 °C (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Measuring Condition
		min.	typ.	max.		
Drop voltage[1]	V_{dr}	–	250	500	mV	I_Q = 300 mA $V_{dr} = V_I - V_Q$
Load regulation	ΔV_Q	–	15	30	mV	I_Q = 5 mA to 400 mA
Line regulation	ΔV_Q	– 15	5	15	mV	ΔV_I = 8 V to 32 V I_Q = 5 mA
Power supply ripple rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp
Temperature output voltage drift	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–

Reset Timing D and Output RO

Reset switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	–
Reset output low voltage	V_{ROL}	–	0.2	0.4	V	$R_{ext} \geq 5\ k\Omega$; V_Q > 1 V
Reset output leakage current	I_{ROH}	–	0	10	µA	V_{ROH} = 5 V
Reset charging current	$I_{D,c}$	3.0	5.5	9.0	µA	V_D = 1 V
Upper timing threshold	V_{DU}	1.5	1.8	2.2	V	–
Lower timing threshold	V_{DRL}	0.2	0.4	0.7	V	–
Reset delay time	t_{rd}	10	16	22	ms	C_D = 47 nF
Reset reaction time	t_{rr}	–	0.5	2	µs	C_D = 47 nF

[1] Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

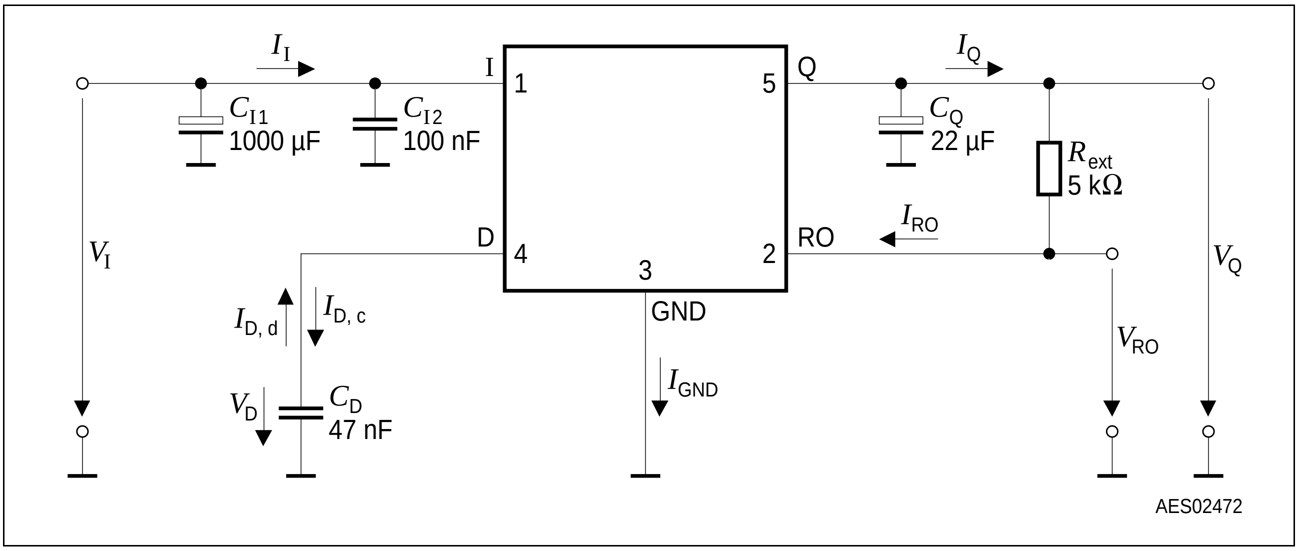


Figure 3 Test Circuit

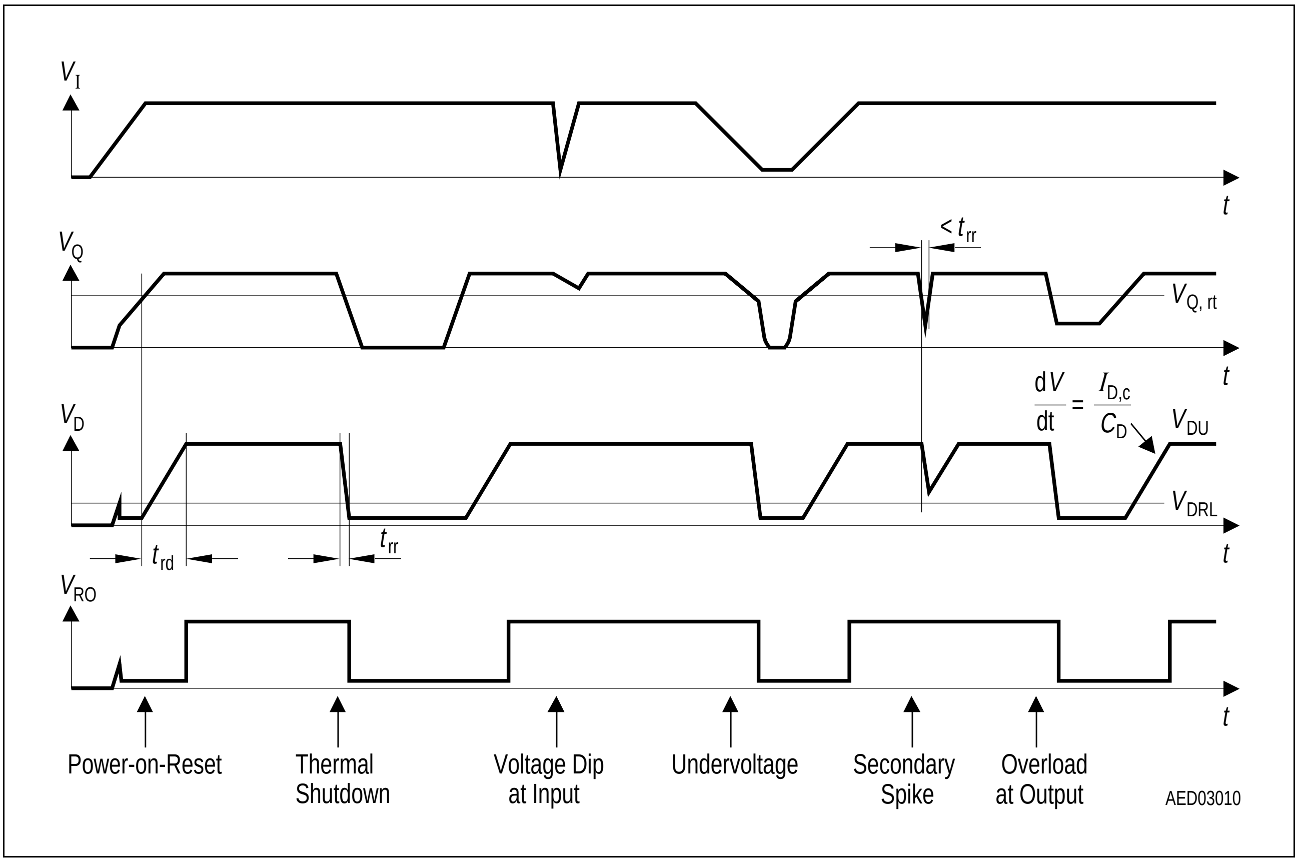
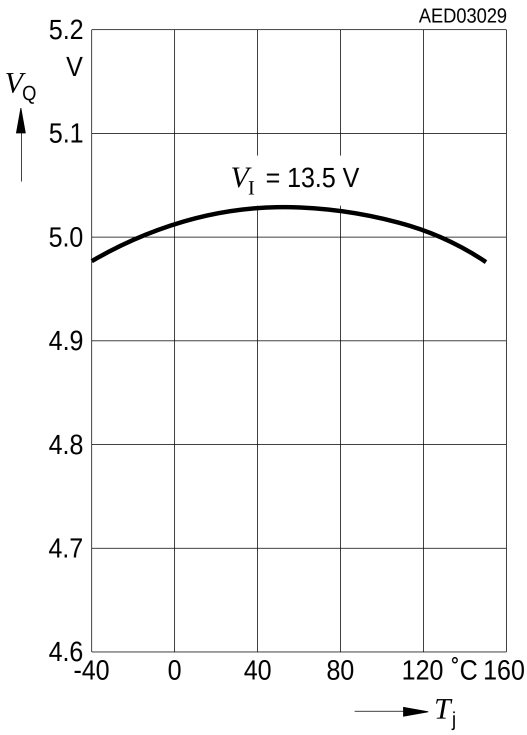
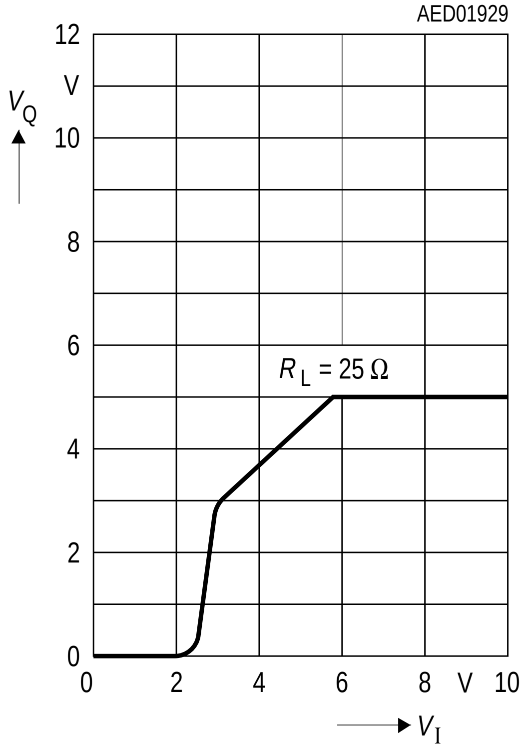


Figure 4 Reset Timing

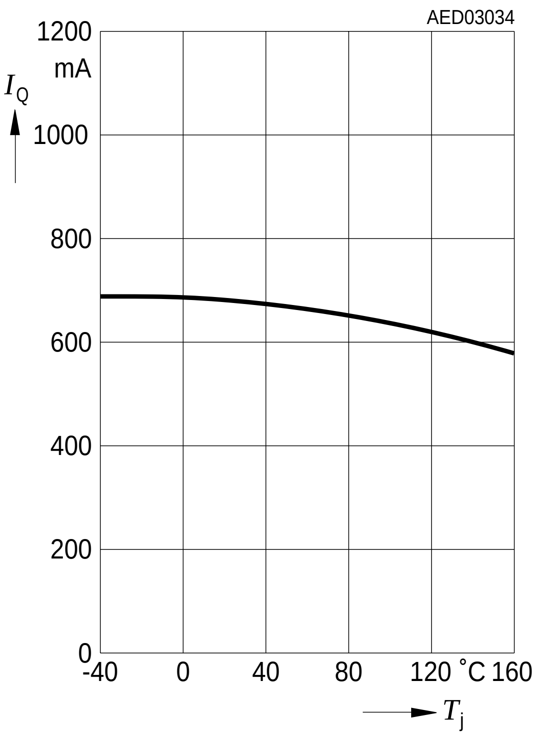
Output Voltage V_Q versus Temperature T_j



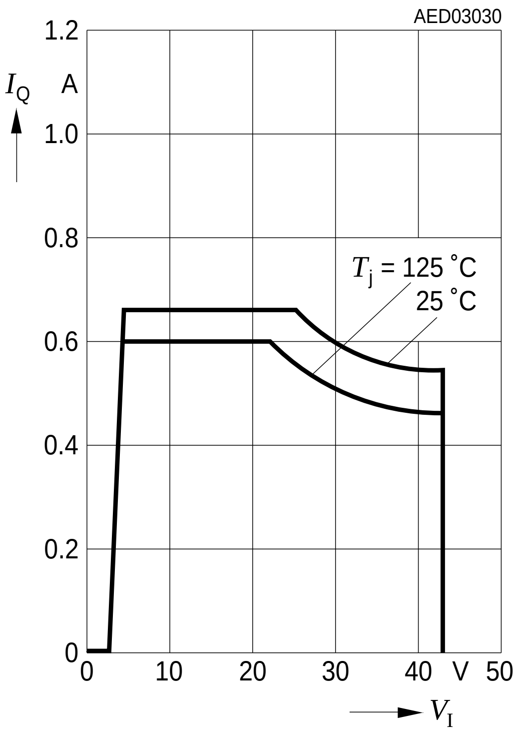
Output Voltage V_Q versus Input Voltage V_I



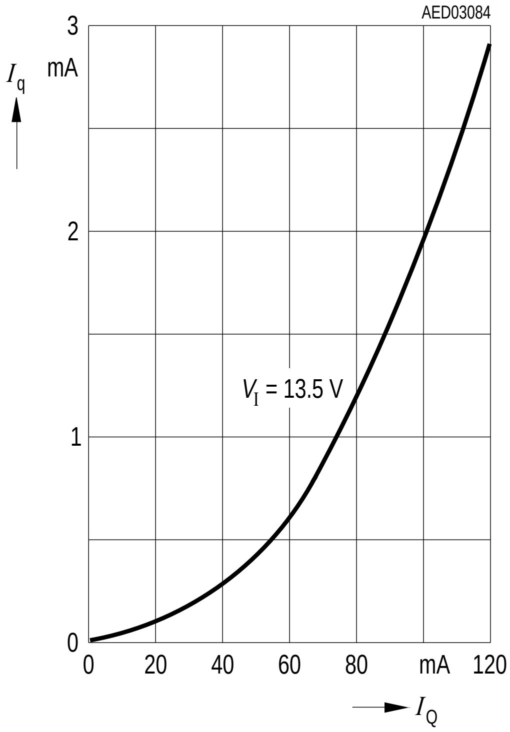
Output Current I_Q versus Temperature T_j



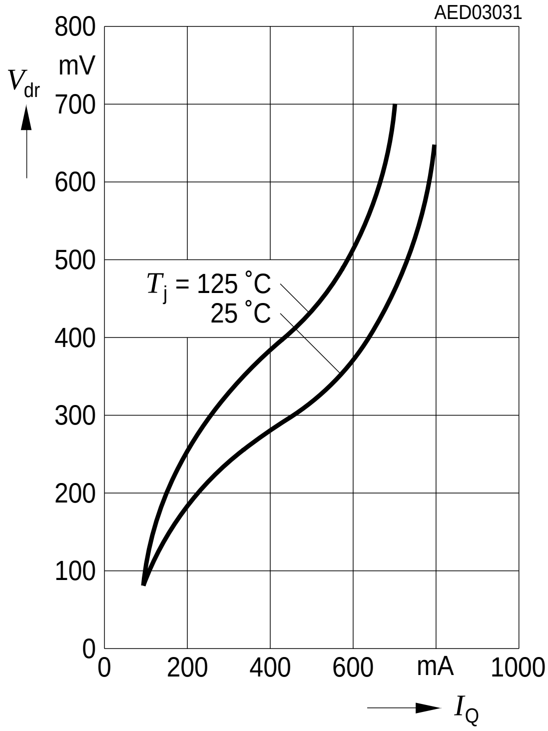
Output Current I_Q versus Input Voltage V_I



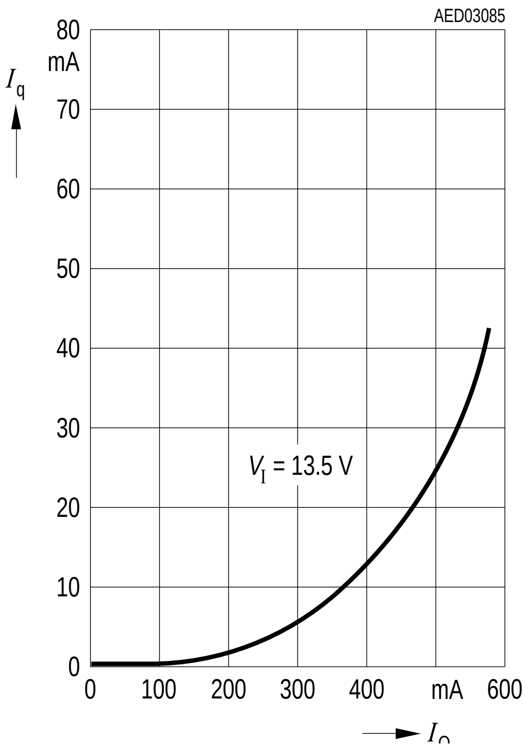
Current Consumption I_q versus Output Current I_Q



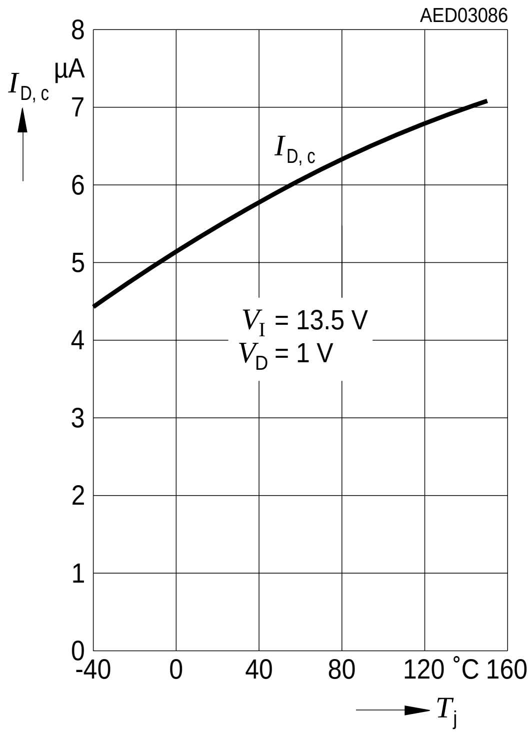
Drop Voltage V_{dr} versus Output Current I_Q



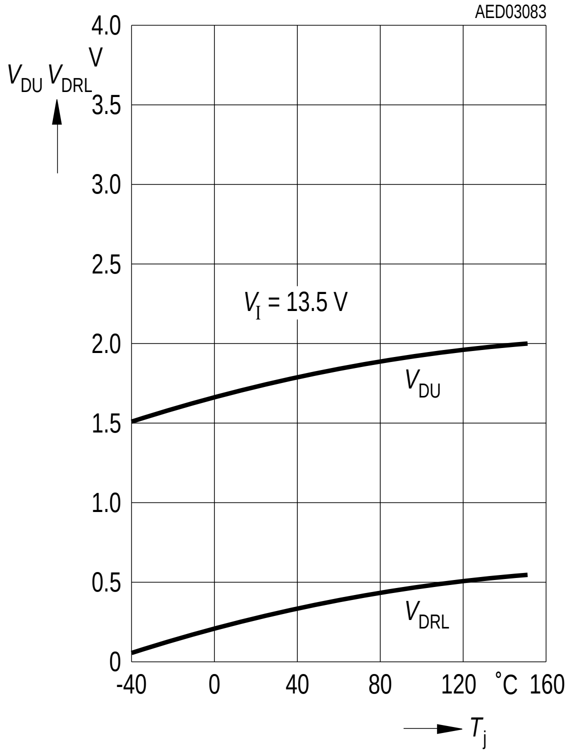
Current Consumption I_q versus Output Current I_Q



Charge Current $I_{D,c}$ versus Temperature T_j

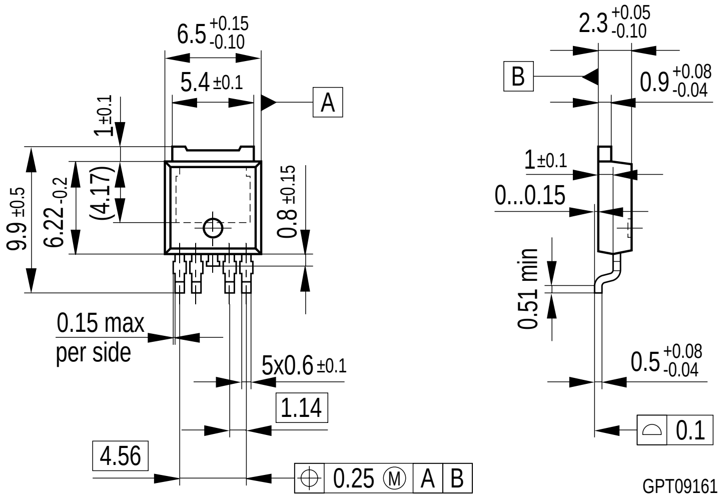


Delay Switching Threshold V_{DU}, V_{DRL} versus Temperature T_j



Package Outlines

P-TO252-5-1 (D-PAK)
(Plastic Transistor Single Outline)



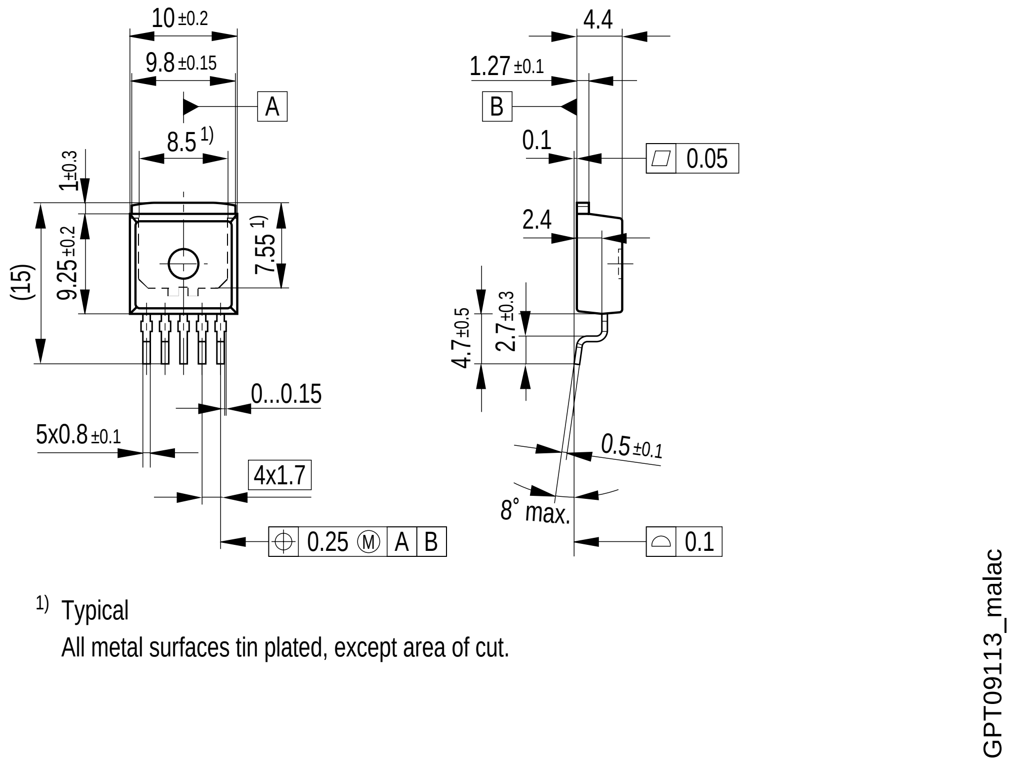
All metal surfaces tin plated, except area of cut.

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

P-TO263-5-1 (SMD)
(Plastic Transistor Single Outline)



1) Typical
All metal surfaces tin plated, except area of cut.

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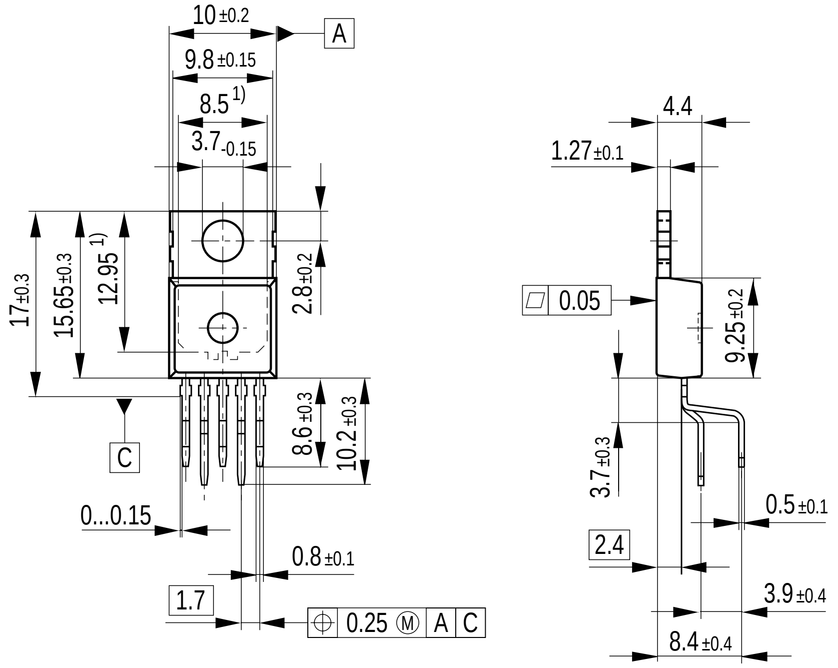
SMD = Surface Mounted Device

Dimensions in mm

P-TO220-5-11
(Plastic Transistor Single Outline)



1) Typical
All metal surfaces tin plated, except area of cut.

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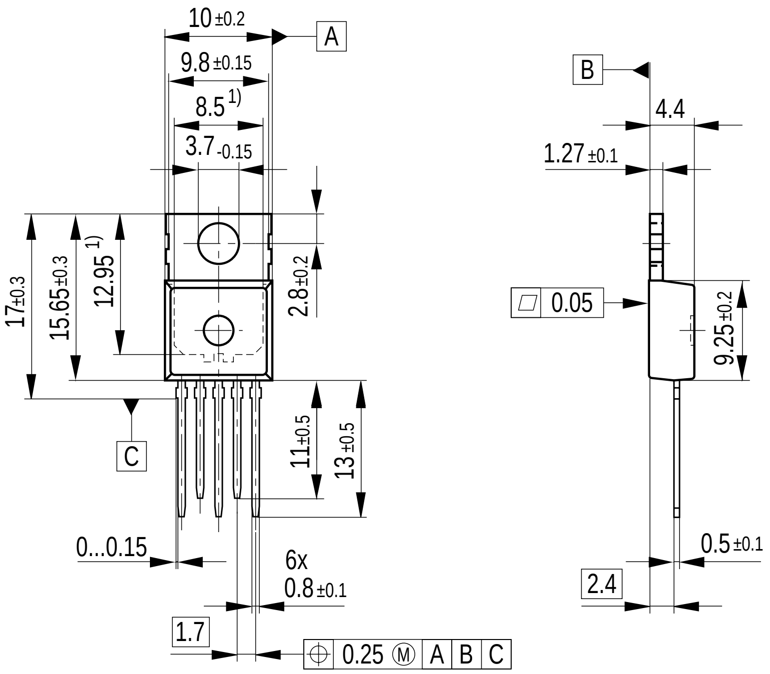
Dimensions in mm

P-TO220-5-12
(Plastic Transistor Single Outline)



Typical
1) All metal surfaces tin plated, except area of cut.

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Sorts of Packing

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Dimensions in mm

Edition 2001-04-24

Published by
Infineon Technologies AG i. Gr.,
St.-Martin-Strasse 53
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